REMARKS

Reconsideration and allowance of the above-referenced application are respectfully requested.

Upon entry of this amendment, claims 1, 3, and 5-32, as amended, will remain in the application.

Claim Rejections – 35 USC § 102

Claims 1, 3, 5, 6, 19, 22, 23, and 25-29 were rejected under 35 U.S.C. 102(b) as being allegedly anticipated by Crouch et al. (U.S. Patent No. 5,995,731, hereinafter "Crouch"). Applicant teaches a tiered memory testing architecture including a first tier in which a single, centralized BIST controller is used to control memory tests on multiple memories by issuing generalized commands to sequencers at a second tier, each sequencer associated with memory modules sharing a common clock domain. At the third tier, memory interfaces, each associated with a corresponding memory module, handle specific interface requirements for each memory module, e.g., based on the specific timing requirements and physical characteristics of the memory modules. Advantages of this hierarchical BIST architecture is that area is conserved and overhead for the BIST controller only happens once, whether for testing a couple of memory modules or dozens.

Crouch in fact teaches away from the approach taught by Applicant. The system proposed by Crouch provides a single BIST controller for each memory module. As described in the Abstract, "Multiple memory arrays (215, 225) in embedded applications are tightly coupled to their own Built-In Self-Test (BIST) controller to form BISTed memory cells (210, 220) supporting structural and retention testing." (emphasis added). All of the systems proposed by Crouch in FIGS. 2-4 have this type of one-to-one "BISTed" memory architecture. The system shown in FIG. 1 is a prior art system criticized by Crouch as not suitable for scaling to the submicron range (col. 5, lines 45-50). There is no indication that the memories 140, 150 coupled to the central BIST controller 130 have different clock domains or physical characteristics, and in fact could not function if they were as there is no intervening structures such as those taught by Applicant to account for such differences.

The Action states on page 17 in the Response to Arguments section that Applicant does not specify a single BIST controller for issuing commands for testing multiple memory modules in the claims. Applicant disagrees. Claims 23 (prior to amendment) and 27 clearly recite "a [] BIST controller" for testing a "plurality" or "set of" memory modules. The antecedent "a" clearly relates to one BIST and terms "plurality" and "set of" to multiple memory modules, differentiating the claimed system from that described in FIGS. 2-4 of Crouch. The recited one BIST controller tests multiple memory modules having different timing requirements and/or physical characteristics, thereby differentiating the claimed system from the prior art system described in FIG. 1 of Crouch. However, the claims have been amended to more clearly recite this feature.

As amended, each of independent claims 1, 23, 25, and 27 recite a single BIST controller for issuing commands for testing multiple memory modules. Crouch does not describe such a system, but rather a typical BIST architecture in which a BIST controller is provided for each memory module and a prior art system in which one BIST controller is used to control memory modules having a common clock domain and physical characteristics. Accordingly, Applicant submits that these claims and their dependencies are allowable.

Claim Rejections – 35 USC § 103

Claims 7-18, 20, 21, 24, 30, and 31 were rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over Crouch in view of Johnston et al. (U.S. Patent No. 6,272,588, hereinafter "Johnston").

Claims 7-18, 20, 21, 24, 30, and 31 depend respectively from one of allowable independent claims 1, 23, 25, and 27. Accordingly, Applicant submits that these claims are allowable with their base independent claims for the reasons stated above and for their additional limitations.

CONCLUSION

In light of the amendments contained herein, Applicants submit that the application is in condition for allowance, for which early action is requested.

Please charge any fees or overpayments that may be due with this response to Deposit Account No. 17-0026.

Respectfully submitted,

Dated: 4/25/06

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